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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,361	02/21/2002	Zoran Krivokapic	G0639	9678

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EXAMINER	
DEO, DUY VU NGUYEN	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,361	KRIVOKAPIC ET AL.	
	Examiner	Art Unit	
	DuyVu n Deo	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *13-24* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/1/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-8, 11, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang (US 5,567,966) and Xiang et al. (US 6,342,414).

Hwang describes a SOI MOSFET comprising: a layer of semiconductor material 2 disposed over an insulating layer 4, which is disposed over a Si substrate (fig. 1 and fig. 6); a source and drain formed from the layer material 2 (figs 5, 6, col. 2, line 10-32); a body formed from the layer material 2 and disposed between the source and drain, the body thickness, about 60m, is less than a thickness of the source and drain, at 200 nm, such that a recess is formed in the layer of the semiconductor material over the body (fig. 6, col. 2, line 29-33); a gate is formed at least in part in the recess and spaced apart from the body by a gate dielectric 14 (figs 4-6).

Since the oxide layer 7 is formed from the layer material 2 (col. 1, line 45-60), it is considered to be a part of the layer material 2. Therefore, etching the oxide 7 would read on claimed the layer of semiconductor material is etched such that the body thickness is less than the source/drain thickness (figs. 3 and 6). Unlike claimed invention, Hwang doesn't describe using a high-K gate dielectric layer. Xiang teaches of using high-K dielectric layer for the gate dielectric (col. 5, line 38-58). It would have been obvious for one skilled in the art at the time of

the invention to modify Hwang in light of Xiang because Xiang teaches that the high-K dielectric provides better electrical coupling with the gate and the channel (col. 5, line 48-53).

Referring to claims 3, 4, and 6, Hwang shows the spacers are formed adjacent and at least in part in the recess and separated from the source/drain 24 by the gate dielectric layer (fig. 5 and 6).

Referring to claims 11 and 12, the high-K dielectric material taught by Xiang includes HfO2, ZrO2 (col. 5, line 43-45).

Referring to claim 7, Xiang shows that the high-K gate dielectric 30 is formed between the spacers and the gate electrode 18 (fig. 15).

Referring to claim 8, Xiang further teaches that the gate electrode include metal containing material (col. 2, line 25-33; col. 6, line 8-10, 24-25).

Referring to claim 2, Hwang doesn't describe the body has a thickness of less than about 50 angstroms. However, he describes that the SOI MOSFET is an experimental test structure (col. 2, line 27). Therefore, at the time of the invention, it would have been obvious for one skilled in the art to determine the desired thickness of the body through routine experimentation in order to provide optimum body thickness for forming the MOSFET with a reasonable expectation of success.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang and Xiang as applied to claim 3 above, and further in view of Parrillo (US 4,951,100).

Unlike claimed invention, applied prior art above doesn't describe the spacers is formed from an updoped polycrystalline silicon. Parrillo describes an MOS structure where the spacers include polysilicon (col. 3, line 32-35, line 65-col. 4, line 3). It would have been obvious for one skilled in the art to modify applied prior art above in light of Parrillo by having the polysilicon in the spacers because it can be shields to prevent the electrons from adversely affecting the mobile carriers in drain region (col. 4, line 1-20).

4. Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang and Xiang as applied to claim 8 above, and further in view of Gardner et al. (Us 6,100,204).

Referring to claim 9, Gardner further shows that the gate electrode can be formed from either polysilicon or aluminum. Therefore, at the time of the invention, it would be obvious to one skilled in the art at either one would be used to form gate electrode with a reasonable expectation of success.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang and Xiang as applied to claim 1 above, and further in view of Misra et al. (US 5,960,270).

Hwang further describes the structure includes a source contact and drain contact over the source/drain. However, he is silent about having a TEOS oxide layer over the source/drain contacts. Misra teaches a MOS structure having a TEOS oxide layer over the source/drain contacts (col. 9, line 45-61). It would have been obvious for one skilled in the art at the time of the invention in light of Misra to have a TEOS oxide layer over the source/drain contacts because Misra teaches that it would form the inter-level dielectric (col. 9, line 61) with a reasonable expectation of success.

Drawings

6. The drawings are objected to under 37 CFR 1.83(a) because they fail to show reference #26 as described in page 4 of the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-12 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-13 of U.S. Patent No. 6,452,229. Although the conflicting claims are not identical, they are not patentably distinct from each other because they both teach a fully depleted SOI FET having a body thickness is smaller than the thickness of source/drain and the gate dielectric is made from high-K material.

Election/Restrictions

9. Applicant's election of claims 1-12 in Paper filed 3/29/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DuyVu n Deo whose telephone number is 571-272-1462. The examiner can normally be reached on 6:00-3:30; with alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DVD
5/5/04